REMARKS

With the foregoing, claim 7 has been canceled without prejudice and incorporated into claim 1. Thus, claims 1-6, and 8-13 are pending and at issue in the above identified patent application. Of the claims at issue, claims 1, and 8 are independent. In view of the foregoing amendments and the following remarks, reconsideration of the application is respectfully requested.

Claim Objections

Claims 7 and 8 were objected to for informal grammatical errors. Claim 7 has been canceled and incorporated into claim 1 with the noted grammatical errors corrected. Claim 8 has also been amended to correct the noted grammatical errors. The foregoing amendment should eliminate any objection to these claims.

The Rejection under 35 U.S.C. § 112

Claims 7 and 8 stand rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. As noted, claim 7 has been canceled, incorporated into claim 1, and amended to clarify that the forming of source/drain regions occurs after the annealing of the substrate to form the re-oxidation layer. Claim 8 has also been amended to clarify that the forming of an LLD structure occurs after the annealing of the substrate done to form the re-oxidation layer. Additionally, claims 1 and 8 have been broadened by eliminating the front face limitation therefrom. The foregoing should eliminate any rejection under 35 U.S.C. §112 that may have been proper.

The Rejections under 35 U.S.C. § 102

Claims 1, 3, 4, and 6 were rejected as anticipated by Tsai et al. (US 5,648,287). It is respectfully submitted that amended claim 1 and all claims dependent thereon are allowable over this patent for at least the reasons set forth below.

As amended, independent claim 1 is directed to a method of manufacturing a semiconductor device including successively depositing gate insulating layer forming material and gate electrode forming material, performing ion-implementation on the substrate including the gate electrode, annealing the substrate to form a re-oxidation layer having a thickness on the substrate which is different from that of the sidewall of the gate electrode, and forming the source/drain region after the annealing of the substrate. In practice, the recited process prevents source/drain ions from diffusing into inappropriate regions during the forming of the source/drain regions.

Tsai et al. does not disclose forming source/drain regions after the annealing of the substrate to form the re-oxidation layer. This fact is admitted on page 7 of the Office action in connection with the rejection of claim 7, which is now incorporated into claim 1. In particular, Tsai et al. discloses a method of forming a MOS transistor including patterning a gate electrode, forming an LDD, forming a sidewall on the side of the gate electrode, forming a highly doped source/drain region, forming an amorphous silicon layer, and implanting nitrogen ions. In other words, Tsai et al. discloses the implantation of nitrogen ions after lightly doped source/drain regions and highly doped source/drain regions have already been formed. As such, the order of manufacturing the MOS transistor is different than the method of claim 1, and as a result, the LDD ions or source/drain ions may be diffused into inappropriate regions during the process of annealing.

Therefore due to the deficiencies in Tsai et al, it follows that Tsai et al. cannot anticipate claim 1 or any claims dependent thereon. In particular, because Tsai et al. does not disclose or suggest forming source/drain regions after the annealing of the substrate, Tsai et al. cannot anticipate claim 1.

Accordingly, for the foregoing reasons, it is respectfully submitted that claim 1 and all claims dependent thereon are in condition for allowance.

Claims 1, 3, 7-8, and 10 were rejected as anticipated by Chiao (US 4,503,601). It is respectfully submitted that amended claims 1, 8 and all claims dependent thereon are allowable over this patent for at least the reasons set forth below.

As noted above, independent claim 1 is directed to a method of manufacturing a semiconductor device including successively depositing gate insulating layer forming material and gate electrode forming material, performing ion-implementation on the surface of the substrate and the gate electrode, annealing the substrate to form a re-oxidation layer having a thickness on the substrate that is different from that of the sidewall of the gate electrode, and forming the source/drain region after the annealing of the substrate. Claim 8 is similar to claim 1, but further recites the forming of an LDD structure after the annealing of the substrate.

Chiao does not disclose performing a nitrogen ion-implementation to a substrate and a gate electrode as recited in claims 1 and 8. In particular, Chiao discloses a manufacturing method of forming a silicon gate including the implantation of a nitrogen ion to form a mask which is patterned, and not to form sidewalls on the gate electrode. Therefore, the nitride layer 16 of Chiao is provided only on the gate electrode 14 as shown in FIG. 4, and not on the substrate as recited by claims 1 and 8. Additionally, the difference in the thickness of the oxide between the side surface of the gate electrode and the source/drain region in Chiao results from the difference of the growth rate of the silicon dioxide between the heavily doped polysilicon (gate electrode) and the lightly doped silicon (substrate) and not from the annealing of the substrate to form a re-

oxidation layer having a thickness on the substrate which is different from that of the sidewall of the gate electrode as recited in claims 1 and 8.

Accordingly, due to the deficiencies in Chiao, it follows that Chiao cannot anticipate claims 1, 8, or any claims dependent thereon. In particular, because Chiao does not disclose or suggest performing a nitrogen ion-implementation to the substrate and the gate electrode, or the annealing of the substrate to form a re-oxidation layer having different thicknesses, Chiao cannot anticipate claims 1 or 8.

Accordingly, for the foregoing reasons, it is respectfully submitted that claims 1, 8 and all claims dependent thereon are in condition for allowance.

The Rejections Under 35 U.S.C. § 103

Claims 7-8, 10-11, and 13 were also rejected as being unpatentable over Tsai et al. in view Chiao. It is respectfully submitted that all claims are allowable over these patents for the reasons set forth below.

Again, as described above, independent claims 1 and 8 are directed to a method of manufacturing a semiconductor device including successively depositing gate insulating layer forming material and gate electrode forming material, performing ion-implementation on the substrate including the gate electrode, annealing the substrate to form a re-oxidation layer having a thickness on the substrate which is different from that of the sidewall of the gate electrode, and forming the source/drain region and/or the LDD structure after the annealing of the substrate.

The Office action rejected claims 1 and 8 as unpatentable over the combination of Tsai et al. and Chiao. Tsai et al. admittedly does not disclose a method of forming the source/drain regions or the LDD structure after the annealing of the substrate. This fact is

conceded on page 7 of the Office action, in connection with the rejection of claim 7, which is now incorporated in claim 1.

The Office action seeks to cure the deficiency of Tsai et al. using Chiao. As noted above, Tsai et al. is directed to a method of manufacturing a MOS transistor, wherein the implantation of nitrogen atoms is performed after lightly doped source/drain regions and highly doped source/drain regions have been already formed. In particular, according to Tsai et al., a gate electrode is patterned, an LDD structure is formed, a sidewall is formed, a highly doped source/drain region is formed, an amorphous silicon layer is formed and then nitrogen ions are implanted. The Office action alleged that Chiao discloses the method of forming the source/drain regions of the LDD structure after annealing the substrate, and that one of ordinary skill in the art would be motivated to form the source drain regions or LDD structure of Tsai after annealing the substrate because it allows for fabrication of MOSFETs free from short channel side effects and drain punch through. The Office action simply ignores the fact that the LDD structure of Tsai et al. is already formed by the time Tsai performs any annealing, or why one of ordinary skill in the art would be motivated to form an LDD structure in Tsai again.

The law is quite clear that, "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention, then the teachings of the references are not sufficient to render the claims prima facie obvious." MPEP § 2143.01, citing, In re Ratti, 270 F.2d 810 (C.C.P.A. 1959) (emphasis added). The Office action proposes that Tsai et al. include an additional step of forming source/drain regions after annealing of the substrate to supplement the source/drain regions already formed. Alternatively, the action suggests that the step of forming the source/drain regions can simply be moved to after the annealing process, without regard

to any teachings of Tsai et al., which clearly describes that the formation of the source/drain regions occurs before any annealing process. In either case, because the proposed combination of Tsai et al. and Chiao unmistakably changes the principle of operation of the Tsai et al. invention, the proposed modification of Tsai et al. is improper as a matter of law and cannot render independent claims 1 and 8 obvious.

In particular, as shown in Figs. 2-6, Tsai et al. requires the formation of the source/drain regions prior to annealing. Specifically, as noted by Tsai et al., it is an object of the invention "to provide a method of forming a lightly doped drain MOS transistor which prevents silicon from diffusing over the sidewall spacers." (Col. 4, ll. 10-15). To do this, a gate electrode 18 is used as a mask to allow impurity ions to first form lightly doped source/drain regions 20. (Fig. 2, Col. 6, ll. 33-35). The sidewall spacers 24 are then formed as another mask to allow impurity ions to form highly doped source/drain regions 28, without affecting the already formed lightly doped source/drain regions 20. (Fig. 2, Col. 6, ll.43-56). The substrate is then annealed to form an amorphous silicon layer 32. (Fig. 3, Col. 6, ll. 56-65). The substrate is then subjected to further nitrogen ion implantation (Fig. 3), and oxidation (Fig. 4) to form gate sidewall spacers 36. At this point, any attempt to form the lightly doped source/drain regions 20 or the highly doped source/drain regions 28 would fail, because the formed sidewall spacers 24, the amorphous silicon layer 32, and the gate sidewall spacers would all, either alone or in combination, act as masks to prevent the formation of the doped source/drain regions 20, 28.

Therefore, <u>any</u> attempt to combine the teachings of Chaio (i.e., the formation of source/drain regions after annealing) with the teachings of Tsai et al., would unmistakably changes the principle of operation of the Tsai et al. invention, because to

attempt to form source/drain regions in Tsai et al. after annealing would clearly result in the failure to create the required doped regions because any impurity ion implantation after annealing would necessarily be prohibited by the formed masked regions. Accordingly, the proposed modification of Tsai et al. is improper as a matter of law and cannot render independent claims 1 and 8 obvious

Furthermore, for all of its disclosure, it is respectfully submitted that Tsai et al. does not disclose or suggest the motivation for fabrication of MOSFETs free from short channel side effect and drain punch through. Assuming for the sake of argument that one of ordinary skill in the art would be motivated to form additional source/drain regions and/or LDD structures in Tsai et al. after the annealing of the substrate, simply combining the teachings of Tsai et al and Chiao does not and could not solve the alleged problem of short channel effect. Thus, no combination of Tsai et al. and Chiao can render obvious claims 1, 8, or any claims dependent thereon.

Specifically, as noted in the background of the present application,

> To solve the short channel effect, it would be necessary to perform a horizontal reduction such as a length reduction of a gate electrode and a vertical reduction as well, such as the reductions of a thickness of a gate insulating layer and a depth of a junction of source/drain.

Paragraph [0003].

Considering that the depth of the junction of source/drain as well as the width of the gate electrode must be reduced to solve the short channel effect, the combination of the manufacturing method of Tsai et al. with the manufacturing method of Chiao simply cannot solve the problem. Specifically, no combination of Tsai et al and Chiao can solve the problem of short channel effect because the formation of additional source/drain regions after the annealing of the substrate as taught by Chiao simply cannot affect the

source/drain regions already formed in the manufacturing method of Tsai et al. Therefore, no combination Tsai et al. and Chiao can solve the problem of short channel effect, and it follows that one of ordinary skill in the art would not be motivated to combine the teachings of Tsai et al., and Chiao because the combination does not solve the problem sought to be addressed.

Accordingly, it is respectfully submitted that claims 1 and 8, and any claims dependent thereon, are in condition for allowance.

Conclusion

Reconsideration of the application and allowance thereof are respectfully requested. If there is any matter that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Respectfully submitted,

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